UNIVERSITY OF CALIFORNIA BERKELEY
Electrical Engineering and Computer Sciences

EE140/240A– MIDTERM #1
Linear/Analog Integrated Circuits

Instructor: Dr. Sashank Krishnamurthy

2024/02/16

Name: _____
SID: _____

This exam contains 20 pages (including this cover page) and 5 questions. Total of points is 52. Please write out the final answers to the questions in the boxes adjacent to the questions. Please show all your work in the space provided to work out the problems. Final answers without any work will not be given any credit.
For all the problems in this exam, assume $\mu_n C_{ox} = 0.5\text{mA/V}^2$, $V_{Tn} = 0.3\text{V}$ for the NMOS transistors. Assume $\mu_p C_{ox} = 0.4\text{mA/V}^2$, $V_{Tp} = 0.45\text{V}$ for the PMOS transistors. Also, assume that the channel length modulation parameter $\lambda = 0$, unless otherwise stated. Numbers adjacent to the MOS transistors indicate the (W/L) ratio of the transistors. Assume all capacitors are infinite, unless otherwise stated.

Distribution of Points

Question	Points	Score
1	12	
2	10	
3	13	
4	11	
5	6	
Total:	52	

1. In this question, we will work with a new device, whose characteristic is shown in Fig. 1

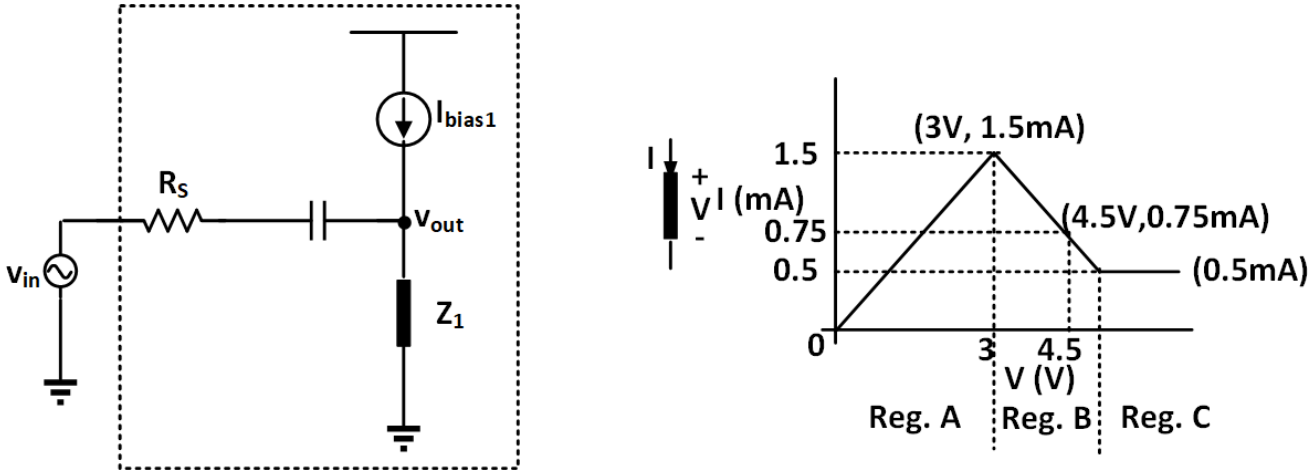

Figure 1: On the left is the circuit for Prob. 1 (a) - 1(c). On the right is the characteristic of the device used for all sub-parts of Prob. 1.

(a) (1 point) In the circuit in Fig. 1, the desired small-signal gain from v_{in} to v_{out} is -2. In what region should we bias the element Z_1?

(b) (3 points) What should the value of R_S be to achieve this small-signal gain of -2?

(c) (4 points) Under the bias condition of part (a) and R_S calculated in part (b), calculate the small-signal 2-port y-parameters for the circuit in the dashed box.

(d) (4 points) Consider the circuit in Fig. 2. Assume that Z_1 is biased in region B, Z_2 is biased in region A, and R_S has the same value as what was computed in part (b). Under this bias condition, what is the small-signal gain v_{in} to v_{out}?

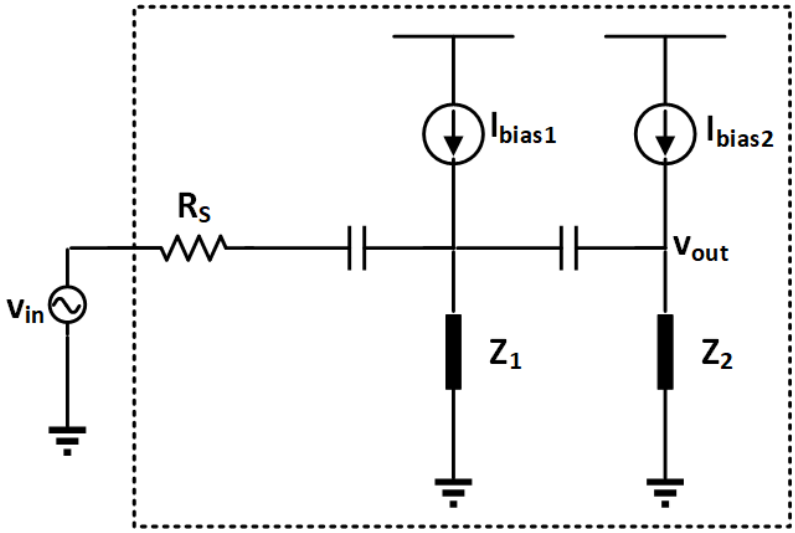

Figure 2: Prob. 1 (d)

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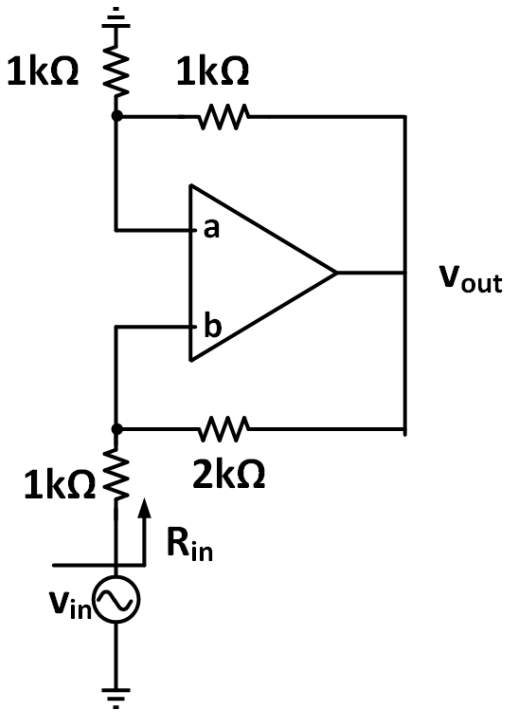

Figure 3: Prob. 2

2. (a) (3 points) Identify the signs on terminal (a) and (b) for the op-amp based circuit in Fig. 3 to be in negative feedback.

(b) (3 points) Assuming that the op-amp is ideal, compute the gain v_{out}/v_{in}.

(c) (4 points) Find the input resistance R_{in} looking into the circuit.

Space to work out problem 2.

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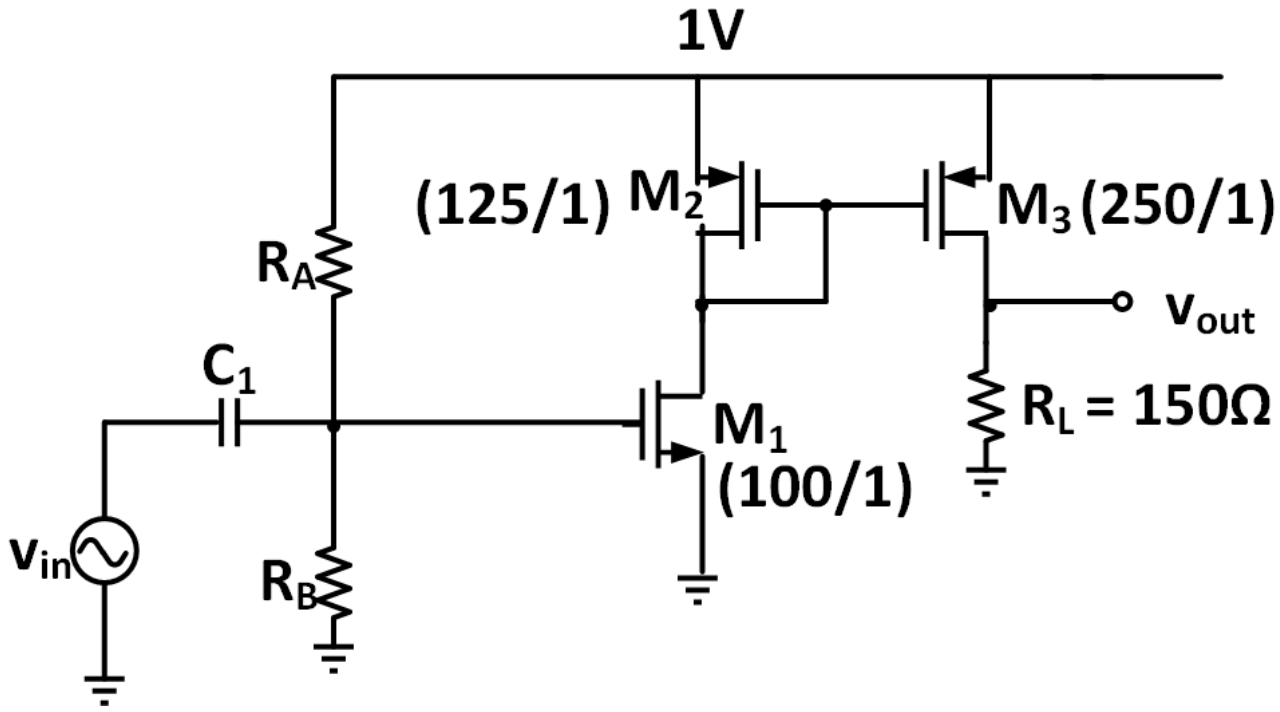

Figure 4: Prob. 3

3. (a) (4 points) $C_1 = \frac{10}{2\pi}$nF. Find the values of R_A, R_B such that the drain current through M_1 and M_2 is 1mA, and the frequency associated with charging/discharging C_1 is 10 times lower than the minimum input frequency of 1kHz. Use the values of R_A, R_B obtained here for subsequent parts.

(b) (4 points) Compute the small-signal gain from v_{in} to v_{out}. In this part, you may assume $C_1 = \infty$.

(c) (5 points) Assume that the input v_{in} is a sinusoid of the form Asin(ω_0t). What is the maximum amplitude A such that all transistors remain in saturation? What limits the maximum swing?

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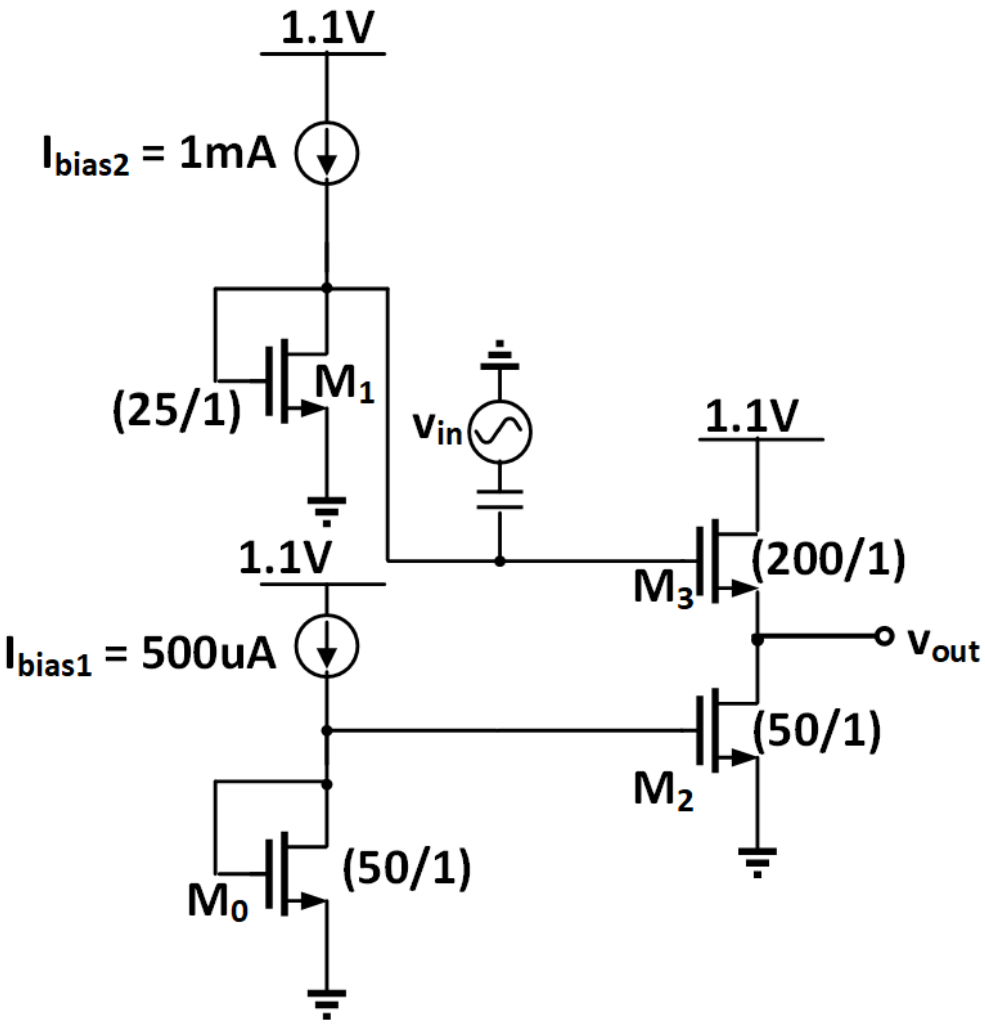

Figure 5: Prob. 4

4. (a) (4 points) Compute the DC operating point of the circuit shown in Fig. 5. That is calculate the DC voltage at the node v_{out}, gate voltages of M_2 and M_3 and the drain current through M_2 and M_3.

(b) (3 points) Compute the small-signal gain from v_{in} to v_{out}.

(c) (4 points) Assume that the input v_{in} is a sinusoid of the form Asin(ω_0t). What is the maximum amplitude A such that all transistors remain in saturation? What limits the maximum swing?

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5. (6 points) The circuit shown in Fig. 6 is biased such that all transistors M_1, M_2, M_3 are in saturation. The small-signal g_m and r_o of the transistors M_1, M_2, M_3 are given by g_{m1}, r_{o1}, g_{m2}, r_{o2}, g_{m3}, r_{o3}, respectively. Calculate the output resistance R_{out} in terms of the small-signal parameters of the transistors g_{m1}, r_{o1}, g_{m2}, r_{o2}, g_{m3}, r_{o3}. You may assume $g_m r_o \gg 1$ for all transistors. V_{G1}, V_{G2} and V_{G3} are the DC bias voltages for M_1, M_2, M_3 respectively.

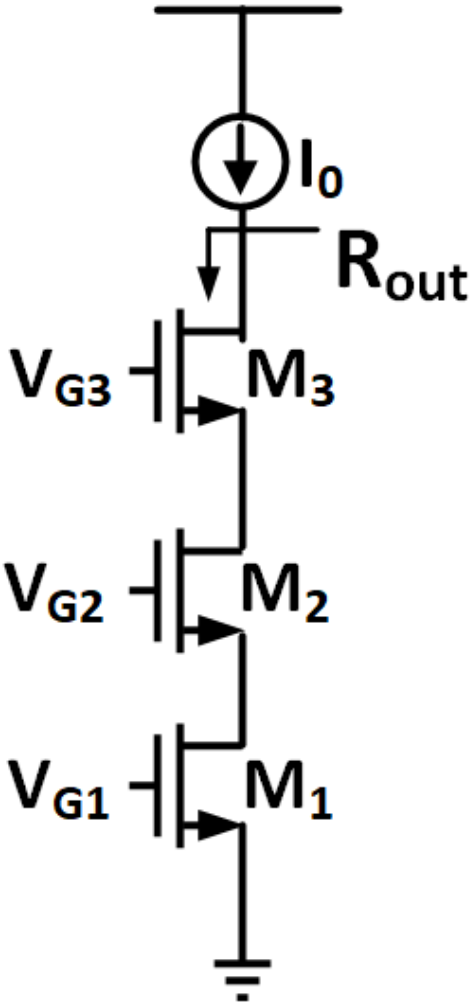

Figure 6: Prob. 5

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