EE140/240A Problem Set 9

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For all the problems in this homework, assume $\mu_n C_{ox} = 0.5\text{mA/V}^2$, $V_{Tn} = 0.3\text{V}$, for the NMOS transistors, assume $\mu_p C_{ox} = 0.4\text{mA/V}^2$, $V_{Tp} = 0.4\text{V}$, for the PMOS transistors. Also, assume that the channel length modulation parameter $\lambda = 0$, unless otherwise mentioned. Numbers adjacent to the MOS transistors indicate the (W/L) ratio of the transistors.

Problem 1. 4+4+2 points Consider the amplifier shown below, which is very similar to the problem 2 in HW8. Assume $V_{DD} = 2\text{V}$, $V_B = 1\text{V}$, $V_{B1} = 0.5\text{V}$. Also, assume that $C_E = 0.2\text{pF}$. Assume $\lambda = \frac{0.2}{\text{V}}$.

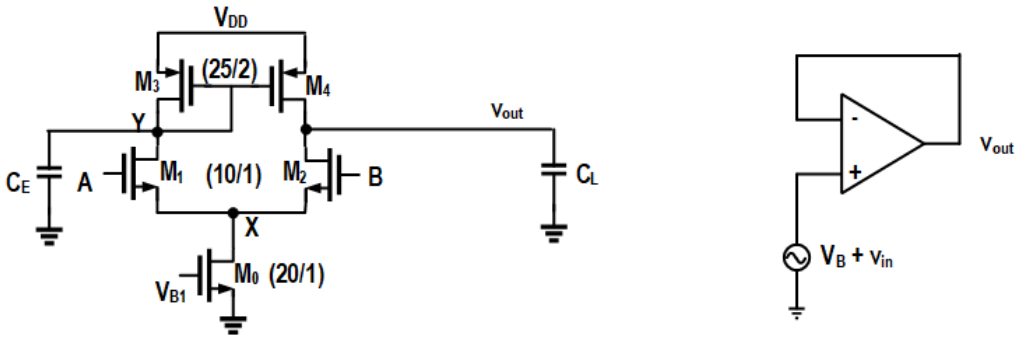

Figure 1: Problem 1

(a) For $C_L = 1\text{pF}$, compute the unity gain frequency and phase margin when the op-amp is connected in unity gain feedback.

(b) For $C_L = 10\text{pF}$, compute the unity gain frequency and phase margin when the op-amp is connected in unity gain feedback. Compare this with the previous part.

(c) For $C_L = 10$pF, what is the maximum slew rate for a rising and falling input step?

Problem 2. 4+4+4+4 points Consider the 2-stage amplifier shown below. Assume $V_{DD} = 2$V, $V_B = 1$V, $V_{B1} = 0.5$V. Also, assume that $C_C = 10$pF. Assume $\lambda = \frac{0.2}{\text{V}}$.

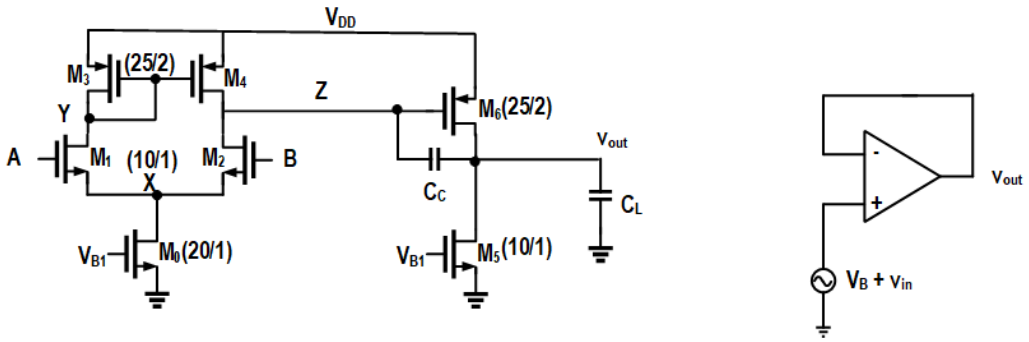

Figure 2: Problem 2

(a) For $C_L = 1$pF, compute the unity gain frequency and phase margin when the op-amp is connected in unity gain feedback.

(b) For $C_L = 10$pF, what is the maximum slew rate for a rising and falling input step?

(c) For $C_L = 10$pF, compute the unity gain frequency and phase margin when the op-amp is connected in unity gain feedback. Compare this with part (a). What comment can you make about the effect of the load capacitance C_L in a 1-stage op-amp and a 2-stage op-amp?

(d) For $C_L = 10$pF, what is the maximum slew rate for a rising and falling input step?

Problem 3. 4+6+2 points Consider the telescopic cascode op-amp shown below. Assume $V_{DD} = 2$V, $V_{B1} = 0.4$V, $V_{B2} = 1$V. Also, assume that $C_L = 10$pF.

(a) Assume that the op-amp is connected in unity gain feedback, and is provided a sinusoidal input of the form Asin(ω_0t). What should be the

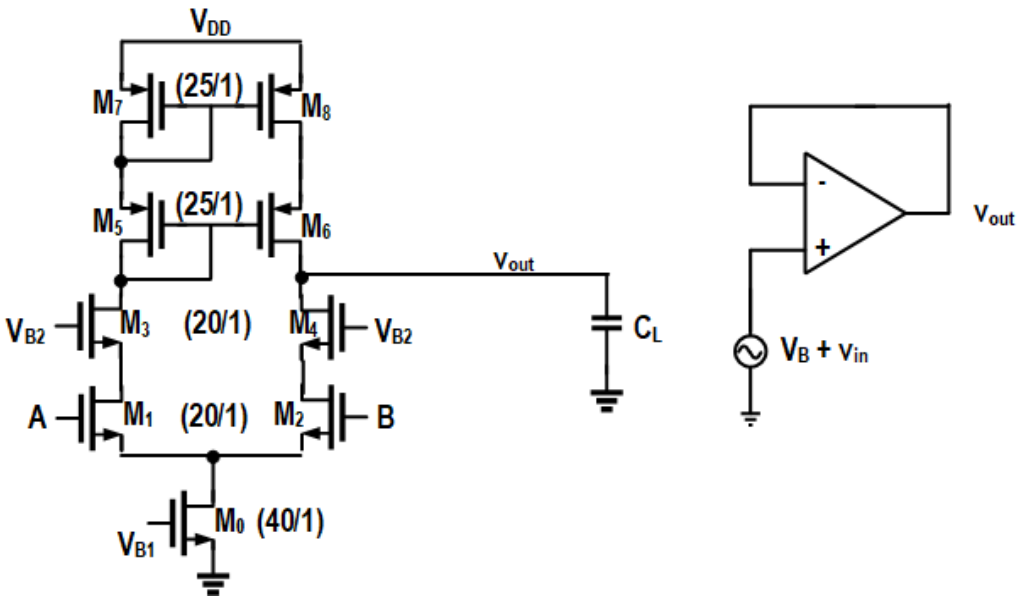

Figure 3: Problem 3

input bias V_B to maximize the output swing? What is the maximum output swing A thus obtained? You may assume $\lambda = 0$ for this part to simplify your calculations.

(b) Find the open-loop differential gain of the op-amp. Use the value of V_B obtained in part (a) as the input bias voltage of transistors M_1, M_2. Assume $\lambda = \frac{0.2}{V}$.

(c) What is the maximum slew rate for a rising and falling input step?

Problem 4. 6+4+3+8 points

Consider the folded cascode op-amp shown below. Assume $V_{DD} = 2$V, $V_{B1} = 0.4$V, $V_{B2} = 1.5$V. Also, assume that $C_L = 10$pF.

(a) Assume that the op-amp is connected in unity gain feedback, and is provided a sinusoidal input of the form Asin(ω_0t). What should be the input bias V_B and the bias voltage V_{B1} to maximize the output swing? What is the maximum output swing A thus obtained? You may assume $\lambda = 0$ for this part to simplify your calculations.

(b) What is the maximum slew rate for a rising and falling input step?

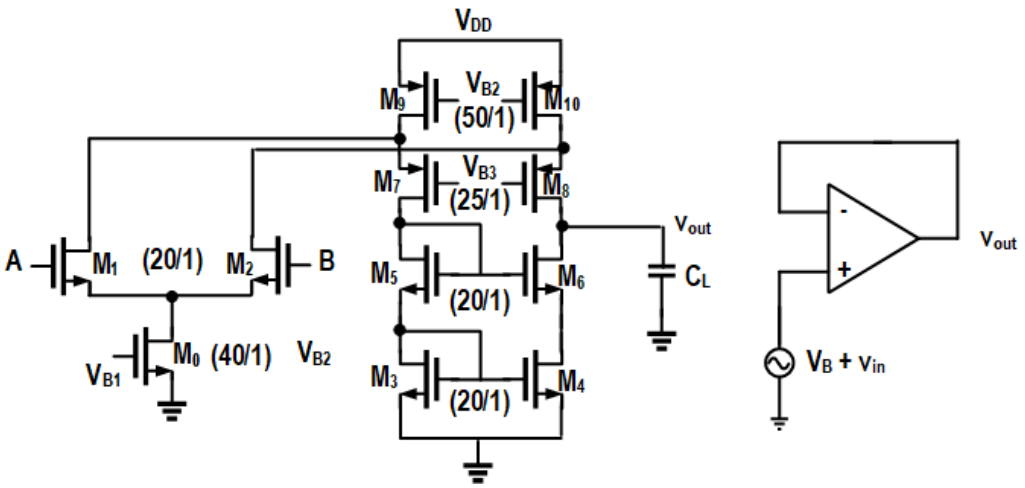

Figure 4: Problem 4

(c) Find the open-loop differential gain of the op-amp. Use the value of V_B obtained in part (a) as the input bias voltage of transistors $\mathrm{M}_1, \mathrm{M}_2$, and V_{B1} as the bias voltage for transistors $\mathrm{M}_7, \mathrm{M}_8$. Assume $\lambda = \frac{0.2}{\mathrm{V}}$.

(d) Now, assume that the sizes of $\mathrm{M}_9, \mathrm{M}_{10}$ are increased to (125/1). Repeat parts (a) and (b) with the new transistor sizes and compare against parts (a) and (b).