EE140/240A Problem Set 7

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For all the problems in this homework, assume $\mu_n C_{ox} = 0.5\text{mA/V}^2$, $V_{Tn} = 0.3\text{V}$, for the NMOS transistors, assume $\mu_p C_{ox} = 0.4\text{mA/V}^2$, $V_{Tp} = 0.4\text{V}$, for the PMOS transistors. Also, assume that the channel length modulation parameter $\lambda = 0$, unless otherwise mentioned. Numbers adjacent to the MOS transistors indicate the (W/L) ratio of the transistors.

Problem 1. 5+3 points In lecture, we analyzed the large-signal behavior of a differential pair. In this question, you will re-derive the same. Please write your answers symbolically in terms of V_{DD}, R_1, I_0, V_{CM}, V_d and $\mu_n C_{ox}$, $\frac{W}{L}$ and V_{Tn}. Assume both M_1 and M_2 have the same $\frac{W}{L}$. Also, assume that V_{DD} is high enough that neither of M_1, M_2 goes into triode.

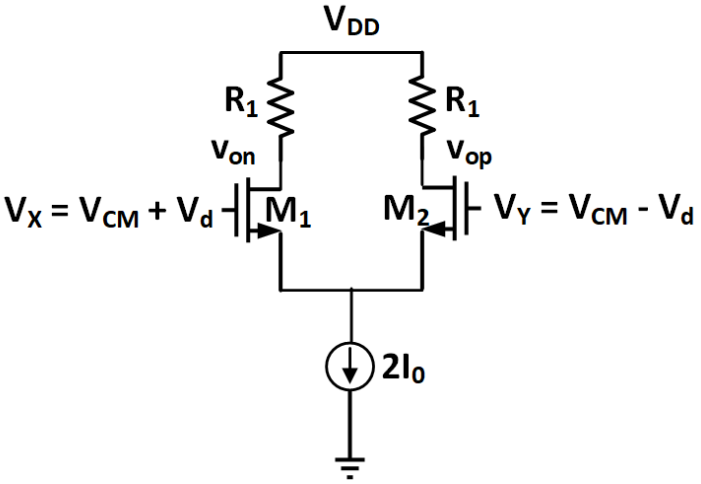

Figure 1: Problem 1

(a) Compute and plot v_{op} and v_{on} as a function of V_d.

(b) Compute and mark the input voltage V_d for which the transistors M_1 and M_2 go into cut-off. What are the corresponding v_{op} and v_{on} values when M_1 and M_2 go into cut-off.

Problem 2. (3+3+2)+(4+4+2)+(4+4+2)+(4+4+2) points For each of the circuits shown below, evaluate the following: i) Differential mode gain $A_{dm} = (v_{op} - v_{on})/v_d$, ii) Common-mode gain $A_{cm} = v_{op}/v_{cm}, v_{on}/v_{cm}$, iii) Common mode rejection ratio (CMRR). Write your answers symbolically in terms of incremental parameters of the transistors g_m and r_o and resistor values, if any. Assume all transistors are in saturation. Other assumptions to be made for each circuit are stated below.

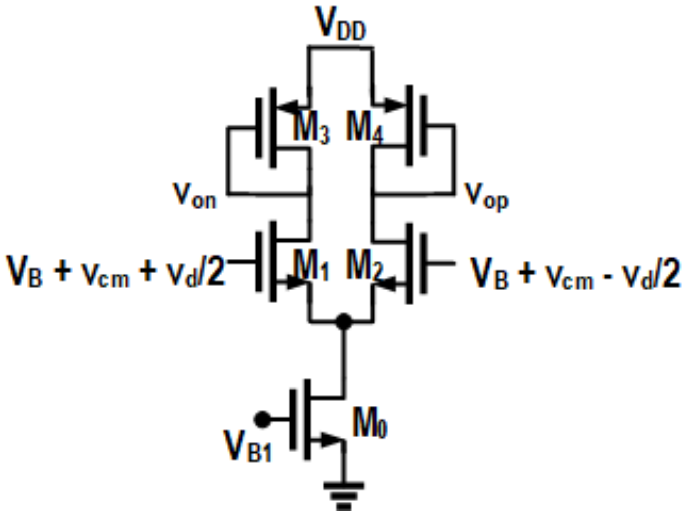

Figure 2: Problem 2(a)

(a) Evaluate A_{dm}, A_{cm} and CMRR for the circuit shown in Fig. 2. Consider channel length modulation for M_0 alone and neglect it for the other transistors. Assume M_1, M_2 have the same size and M_3, M_4 have the same size.

(b) Evaluate A_{dm}, A_{cm} and CMRR for the circuit shown in Fig. 3. Consider channel length modulation for M_0 alone and neglect it for the other transistors. Assume M_1, M_2 have the same size and M_3, M_4 have the same size.

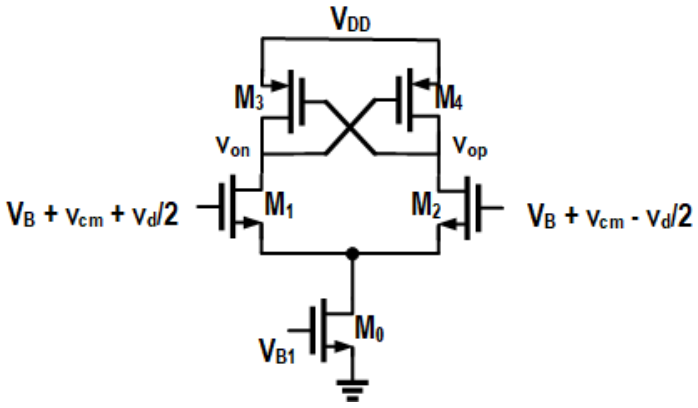

Figure 3: Problem 2(b)

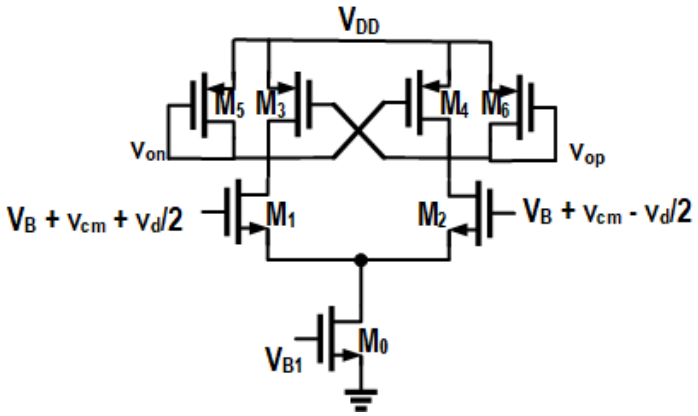

Figure 4: Problem 2(c)

(c) Evaluate A_{dm}, A_{cm} and CMRR for the circuit shown in Fig. 4. Consider channel length modulation for all transistors. Assume M_1, M_2 have the same size and $M_3 - M_6$ have the same size.

(d) Evaluate A_{dm}, A_{cm} and CMRR for the circuit shown in Fig. 5. Consider channel length modulation for M_0 alone and neglect it for the other transistors. Assume M_1, M_2 have the same size and M_3, M_4 have the same size.

Problem 3. (4+2+4+4)+(4+2+4+4)+(4+2+4+4) points For all parts of this problem, assume $V_{DD} = 1.8\text{V}, V_B = 0.9\text{V}, V_{B1} = 0.5\text{V}$. Also, assume

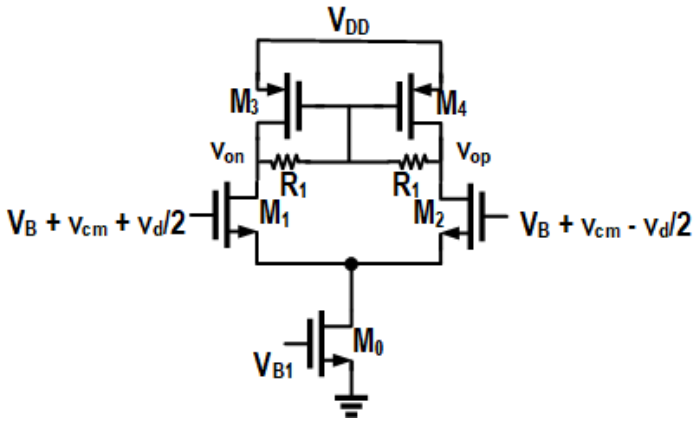

Figure 5: Problem 2(d)

$\lambda_n = \lambda_p = 0.2/\text{V}$.

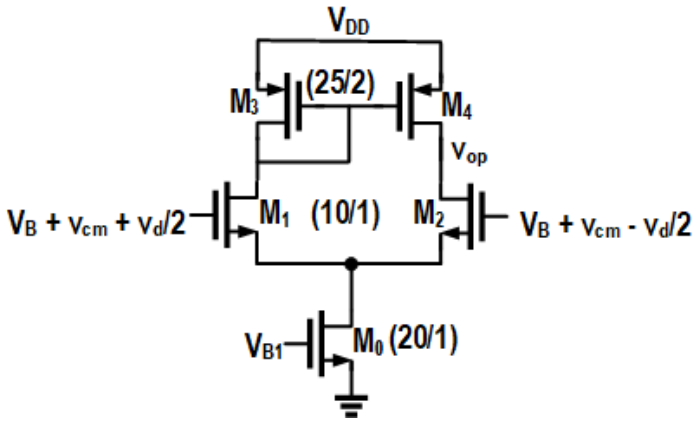

Figure 6: 1-stage op-amp without source follower

(a) For the circuit in Fig. 6, compute the differential mode gain $A_{dm} = v_{op}/v_d$, common-mode gain $A_{cm} = v_{op}/v_{cm}$, the common-mode rejection ratio (CMRR) and the output resistance looking from v_{op}.

(b) Now, the circuit in Fig. 6 is used as an op-amp and configured in unity gain feedback as shown in Fig. 7. Which terminal of the circuit in Fig. 6 is the positive terminal and which is the negative terminal of the op-amp?

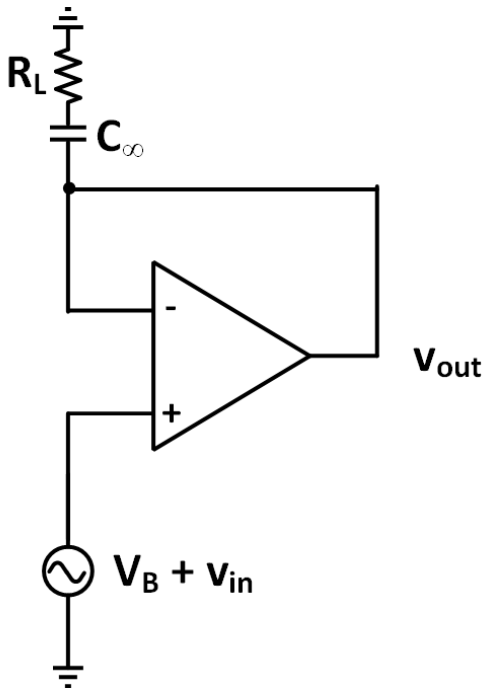

Figure 7: Problem 3: Unity gain opamp

(c) Now, assume $R_L = \infty$. Compute the gain v_{out}/v_{in} of the circuit in Fig. 6 configured in unity gain feedback. Also, compute the output resistance, and compare it with the output resistance without feedback.

(d) Now, assume $R_L = 100\Omega$. Compute the gain v_{out}/v_{in} of the circuit in Fig. 6 configured in unity gain feedback. Comment on what you observe.

(e) Now, we add a source follower to the circuit in Fig. 6 to get the circuit in Fig. 8. Compute the differential mode gain $A_{dm} = v_{op}/v_d$ and the output resistance looking from v_{op}.

(f) The circuit in Fig. 8 is used as an op-amp and configured in unity gain feedback as shown in Fig. 7. Which terminal of the circuit in Fig. 8 is the positive terminal and which is the negative terminal of the op-amp?

(g) Now, assume $R_L = \infty$. Compute the gain v_{out}/v_{in} of the circuit in Fig. 8 configured in unity gain feedback. Also, compute the output

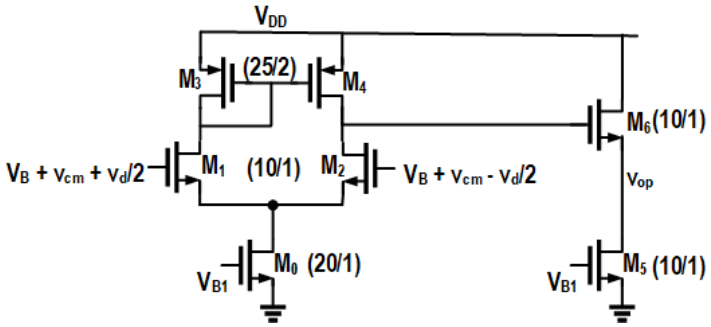

Figure 8: 1-stage op-amp with source follower

resistance, and compare it with the output resistance without feedback.

(h) Now, assume $R_L = 100\Omega$. Compute the gain v_{out}/v_{in} of the circuit in Fig. 8 configured in unity gain feedback. Compare this with the answer obtained in part (d), and give your reasoning.

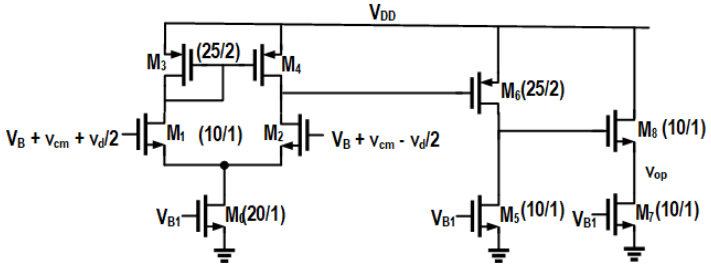

Figure 9: 2-stage op-amp with source follower

(i) Now, we add another gain stage before the source follower to get a two-stage op-amp of Fig. 9. Compute the differential mode gain $A_{dm} = v_{op}/v_d$ and the output resistance looking from v_{op}.

(j) The circuit in Fig. 9 is used as an op-amp and configured in unity gain feedback as shown in Fig. 7. Which terminal of the circuit in Fig. 9 is the positive terminal and which is the negative terminal of the op-amp?

(k) Now, assume $R_L = \infty$. Compute the gain v_{out}/v_{in} of the circuit in Fig. 9 configured in unity gain feedback. Also, compute the output resistance, and compare it with the output resistance without feedback.

(l) Now, assume $R_L = 100\Omega$. Compute the gain v_{out}/v_{in} of the circuit in Fig. 9 configured in unity gain feedback. Compare this with the answers obtained in part (d) and (h), and give your reasoning.