EE140/240A Problem Set 6

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For all the problems in this homework, assume $\mu_n C_{ox} = 0.5\text{mA/V}^2$, $V_{Tn} = 0.3\text{V}$, for the NMOS transistors, assume $\mu_p C_{ox} = 0.4\text{mA/V}^2$, $V_{Tp} = 0.4\text{V}$, for the PMOS transistors. Also, assume that the channel length modulation parameter $\lambda = 0$, unless otherwise mentioned. Numbers adjacent to the MOS transistors indicate the (W/L) ratio of the transistors.

Problem 1. For the cascode amplifier in Fig. 1, assume $C_{gs} = 25\text{fF}$, $C_{gd} = 10\text{fF}$, $C_{db} = 10\text{fF}$, $C_{sb} = 10\text{fF}$. Assume $R_A = R_B$, and $R_S \ll R_A, R_B$. The exact frequency response of this cascode amplifier turns out to be of the form

$$\frac{v_{out}}{v_{in}}(s) = A\frac{1 - \frac{s}{\omega_z}}{1 + as + bs^2 + cs^3} \tag{1}$$

Under certain conditions and at low enough frequencies, we saw that we could approximate the response as,

$$\frac{v_{out}}{v_{in}}(s) \approx A\frac{1 - \frac{s}{\omega_z}}{1 + as} \tag{2}$$

(a) In this part, assume $R_S = 2\text{k}\Omega$, $R_L = 400\Omega$, and $\lambda = 0$. Compute the full frequency response of the form equation (1), and the approximate frequency response of the form equation (2).

(b) Compute the 3-dB bandwidth from both the accurate response (you may use any computational tool for this) and the approximate response. Which time constant dominates the frequency response? Compare this problem to problem 2(a)/2(b) of HW5. What do you observe in terms of which time constant dominates the frequency response, and the location of the zero?

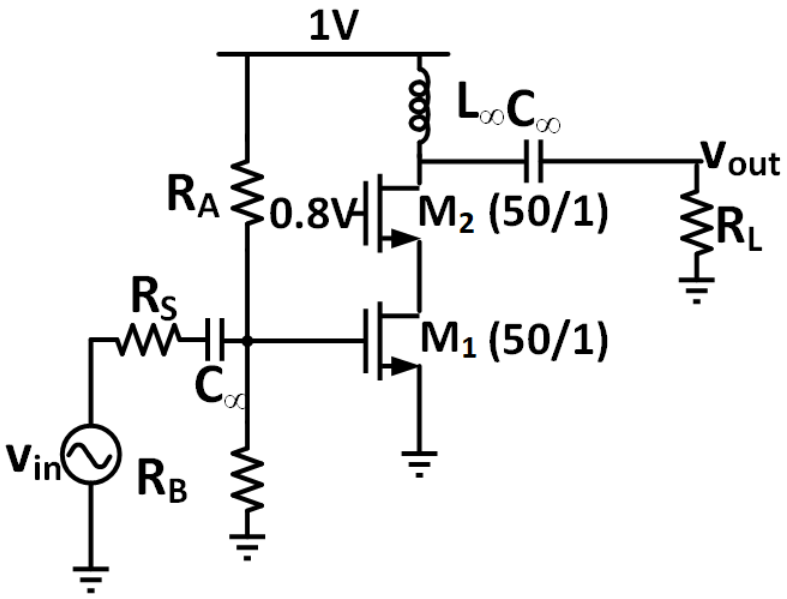

Figure 1: Problem 1

(c) In this part and the subsequent part, assume $R_S = 2\text{k}\Omega$, $R_L = 20\text{k}\Omega$, and $\lambda = 0$. Compute the full frequency response of the form equation (1), and the approximate frequency response of the form equation (2).

(d) Compute the 3-dB bandwidth from both the accurate response (you may use any computational tool for this) and the approximate response. Which time constant dominates the frequency response? Compare this problem to problem 2(c)/2(d) of HW5. What do you observe in terms of which time constant dominates the frequency response, and the location of the zero?

Problem 2. In lecture, we saw a PMOS common source amplifier with an NMOS active load. Now, we will consider the following NMOS common source amplifier with a PMOS active load (Fig. 2). Assume $\lambda = 0.1/V$ for this question. You may ignore λ for easier DC bias point calculations.

(a) For what bias voltage V_G will we have both transistors M_1 and M_2 to be in saturation? What is the range of DC voltages V_{out} such that both M_1 and M_2 are in saturation?

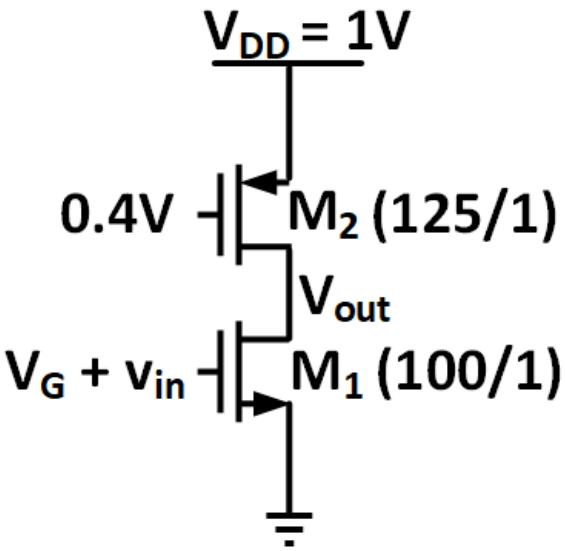

Figure 2: Problem 2

(b) Assuming, both M_1 and M_2 are in saturation, what is the small-signal gain v_{out}/v_{in}.

(c) Compute the large-signal V_G v/s V_{out} characteristics similar to what was derived in lecture for the PMOS common-source amplifier. Analytically, compute the V_{out} as a function of V_G in the different operating regions. You may use the small-signal approximation just for the region where both are in saturation. Mark different relevant points on the curve, where transistors transition into different operating regions.

(d) Fig. 3 shows a complete circuit of Fig. 2, including a source resistance $R_S = 1\text{k}\Omega$ and a feedback resistor R_{big} for stable biasing. What should the value of R_{big} be to ensure that it does not affect the small-signal gain computed in part (b)?

Problem 3. Consider the inverter circuit shown in Fig. 4. The symbol of the inverter is also shown.

(a) Compute the trip point voltage of the inverter V_G^* in terms of $(\mu C_{ox})_p$, $(\mu C_{ox})_n$, V_{Tp}, V_{Tn}, V_{DD}, $(W/L)_p$ and $(W/L)_n$.

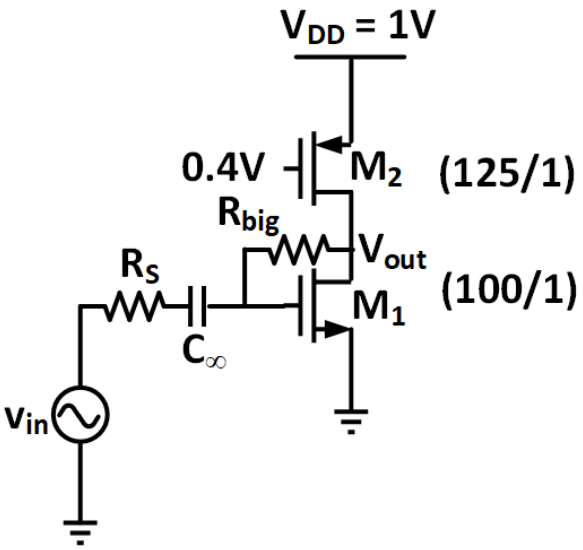

Figure 3: Problem 2(d)

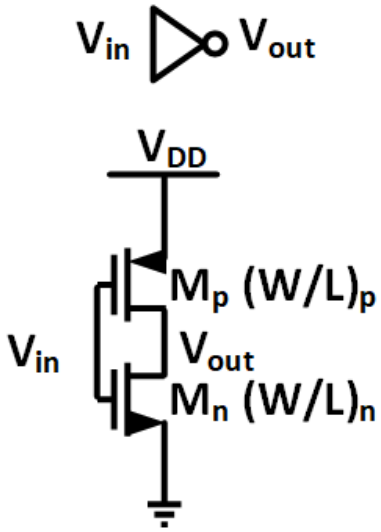

Figure 4: Problem 3

(b) Assuming that we want a drain current of 1mA, and a trip point voltage $V_G^* = 0.5$V, what should the sizes of the NMOS and PMOS transistor be? You may assume a supply voltage $V_{DD} = 1.1$V.

(c) Plot the V_{in} v/s V_{out} characteristics for the inverter in part (b). Assume $\lambda = 0$ for both NMOS and PMOS transistors. Analytically, compute the V_{out} as a function of V_G in the different operating regions. Mark different relevant points on the curve, where transistors transition into different operating regions.

Problem 4. Consider the circuit shown in Fig. 5. A 1x inverter is the inverter from Question 3(b). A 2x inverter has NMOS and PMOS transistors of twice the size. Assume $\lambda_p = \lambda_n = 0$, and $R_S = 2\text{k}\Omega$. Assume $C_1 = 10\text{fF}$, $C_2 = 25\text{fF}$, $C_3 = 10\text{fF}$.

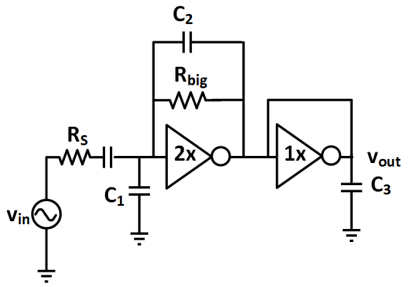

Figure 5: Problem 4

(a) What is the purpose of R_{big}? Assuming R_{big} is infinite, compute the small-signal gain from v_{out}/v_{in} at really low frequencies. You may neglect the capacitances for this question.

(b) What amplifier is this, and what is the purpose of the 1x inverter?

(c) Compute the full-frequency response $v_{out}/v_{in}(s)$. You may use results from previous homework, with detailed justification.

Problem 5. Consider the differential amplifier shown in Fig. 6. Assume that the devices are all biased in saturation. Compute the following in terms of incremental parameters (g_m, r_o) of the respective transistors and the resistors R_1, R_2. Assume that M_1 and M_2 have identical sizes. V_B, V_{B1} are gate bias voltages for the respective transistors. v_{cm} and v_d are small-signal common mode and differential mode inputs, respectively.

(a) What is the differential mode gain $(v_{op} - v_{on})/v_d$?

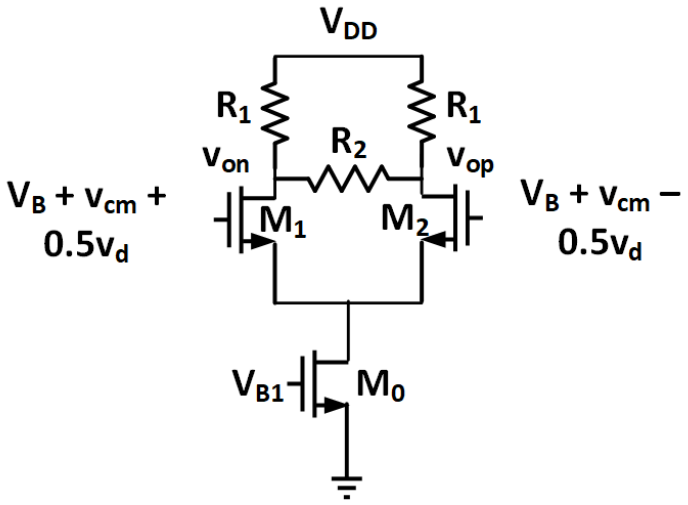

Figure 6: Problem 5

(b) What is the common mode gain v_{op}/v_{cm}, v_{on}/v_{cm}?

(c) What is the common mode rejection ratio (CMRR)?