EE140/240A Problem Set 2

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Due: Feb 5, 2024

For all the problems in this problem set, assume $\mu_n C_{ox} = 0.5\text{mA/V}^2$, $V_{Tn} = 0.3\text{V}$, and the channel length modulation parameter $\lambda = 0$. Numbers adjacent to the MOS transistors indicate the (W/L) ratio of the transistors.

Problem 1. MOS operating points and V/I curves **3+3 points**
Assume that the (W/L) of the NMOS transistor is 40/1.

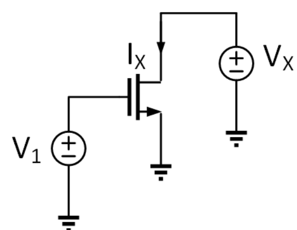

Figure 1: Problem 1

(a) Assume $V_1 = 0.5\text{V}$ in Figure 1. Calculate and sketch the I_X versus V_X characteristic as V_X varies from 0V to 1V. Identify the different operating regions of the transistor.

(b) Assume $V_X = 1\text{V}$ in Figure 1. Caculate and sketch the I_X versus V_1 characteristic as V_1 varies from 0V to 1V. Identify the different operating regions of the transistor.

Problem 2. 3+2+3+3+4 points Assume $R_S = 200\Omega$, $R_{L1} = 500\Omega$, $R_L = 500\Omega$. Assume that the capacitors C_1 ,C_2 and C_3 are ideal infinite capacitors where appropriate, and find their values in the other parts.

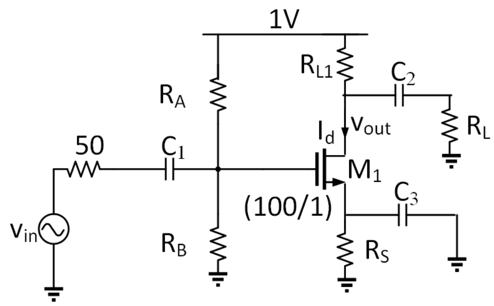

Figure 2: Problem 2

(a) Calculate the ratio of R_A to R_B to ensure that the quiescent I_{DS} = 1mA. Verify if the transistor M_1 is in saturation.

(b) Calculate the small signal gain from v_{in} to v_{out}. For this portion, assume R_A, R_B are much larger than 50Ω.

(c) The minimum frequency of the input v_{in} is 1kHz, and C_1 = 3nF. Based on this and the ratio computed in part (a), calculate the absolute values of R_A and R_B such that the frequency associated with charging/discharging the capacitor C_1 is at least 10 times smaller than the minimum frequency of operation?

(d) Calculate the C_2 such that the frequency associated with charging/ discharging the capacitor C_2 is at least 10 times smaller than the minimum frequency of operation (1kHz)?

(e) **(Compulsory for EE240A, Bonus for EE140)** Calculate the C_3 such that the frequency associated with charging/discharging the capacitor C_3 is at least 10 times smaller than the minimum frequency of operation (1kHz)?

Problem 3. Common source amplifier swing limits. **3+4+3+4+5 points**

Assume $R_A = R_B = 100\text{k}\Omega$ and an ideal infinite capacitor C_∞ for the circuit in Figure 3. In this problem, we will see swing limits before the output node voltage v_{out} exhibits distortion. In lecture, we saw two limitations causing distortion, the output node voltage approaching the supply voltage V_{DD} and the output node voltage going low enough to send the transistor M_1 into triode region.

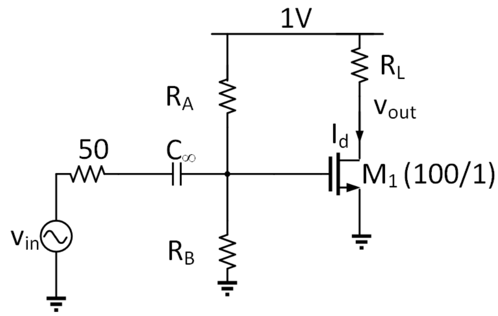

Figure 3: Problem 3

(a) Assume $R_L = 500\Omega$. Compute the DC operating point of the circuit and the small-signal gain v_{out}/v_{in}.

(b) Assume that the input v_{in} is a sinusoid of the form $A\sin(\omega_0 \mathrm{t})$. For the values in part (a), what is the maximum amplitude A before which v_{out} exhibits distortion? What limits the maximum swing?

(c) Now assume $R_L = 200\Omega$. Compute the DC operating point of the circuit and the small-signal gain v_{out}/v_{in}.

(d) Assume that the input v_{in} is a sinusoid of the form $A\sin(\omega_0 \mathrm{t})$. For the values in part (c), what is the maximum amplitude A before which v_{out} exhibits distortion? What limits the maximum swing?

(e) **(Compulsory for EE240A, Bonus for EE140)** What value of R_L maximizes the output swing without distorting the output?

Problem 4. Opamp feedback. 5+5 points
In lecture, we saw the notion of negative and positive feedback. To check if a feedback loop is in negative feedback, we broke the loop, gave a perturbation and observed how the perturbation propagated through the loop and returned to the point where we broke the loop. If what returned was in the opposite direction as the original perturbation, we saw that the feedback loop was in negative feedback. Use this knowledge to solve the following questions based on Figure 4. To perform this perturbation test, assume that the opamp has a large gain A, and to compute the gain, assume that the op-amp is ideal, that is $A = \infty$.

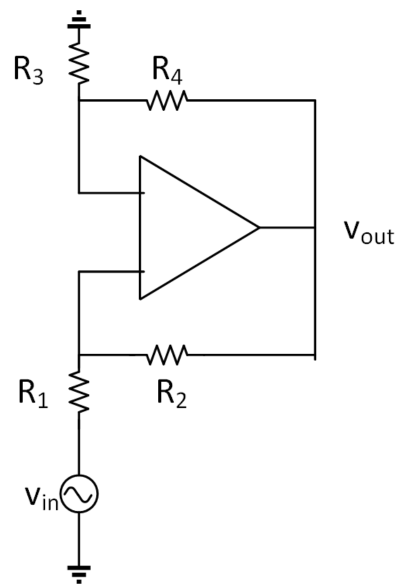

Figure 4: Op-amp feedback

(a) Assume $R_1 = 1k\Omega$, $R_2 = 5k\Omega$, $R_3 = 2k\Omega$, $R_4 = 1k\Omega$. What should the signs on the op-amp be for this circuit to be in negative feedback? Also, compute the gain v_{out}/v_{in}.

(b) Now, assume $R_1 = 4k\Omega$, $R_2 = 5k\Omega$, $R_3 = 1k\Omega$, $R_4 = 2k\Omega$. What should the signs on the op-amp be for this circuit to be in negative feedback? Also, compute the gain v_{out}/v_{in}.