UNIVERSITY OF CALIFORNIA BERKELEY
Electrical Engineering and Computer Sciences

EE140/240A– FINAL EXAM
Linear/Analog Integrated Circuits

Instructor: Dr. Sashank Krishnamurthy

2024/05/08

Name: _____
SID: _____

This exam contains 32 pages (including this cover page) and 5 questions. Total of points is 64. Please write out the final answers to the questions in the boxes adjacent to the questions. Please show all your work in the space provided to work out the problems. Final answers without any work will not be given any credit. You may reuse results and expressions from lecture, homework and textbooks, as long as you clearly state it.
For all the problems in this exam, assume $\mu_n C_{ox} = 0.5\text{mA/V}^2$, $V_{Tn} = 0.3\text{V}$ for the NMOS transistors. Assume $\mu_p C_{ox} = 0.4\text{mA/V}^2$, $V_{Tp} = 0.4\text{V}$ for the PMOS transistors. Also, assume that the channel length modulation parameter $\lambda = 0$, unless otherwise stated. Numbers adjacent to the MOS transistors indicate the (W/L) ratio of the transistors.

Distribution of Points

Question	Points	Score
1	5	
2	10	
3	25	
4	15	
5	9	
Total:	64	

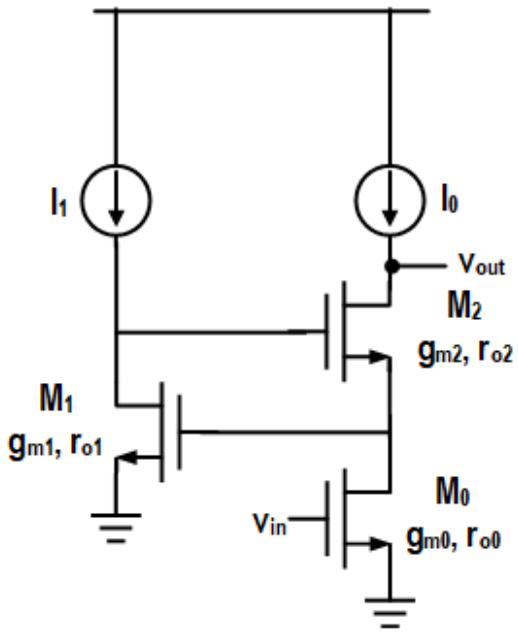


Figure 1: Fig. for Q1

1. (a) (5 points) Compute the small-signal gain v_{out}/v_{in} in terms of the small-signal parameters mentioned adjacent to the transistors. Assume all transistors are in saturation region of operation. *(You may use small-signal analysis to compute the gain.)*

Additional space to work out problem 1.

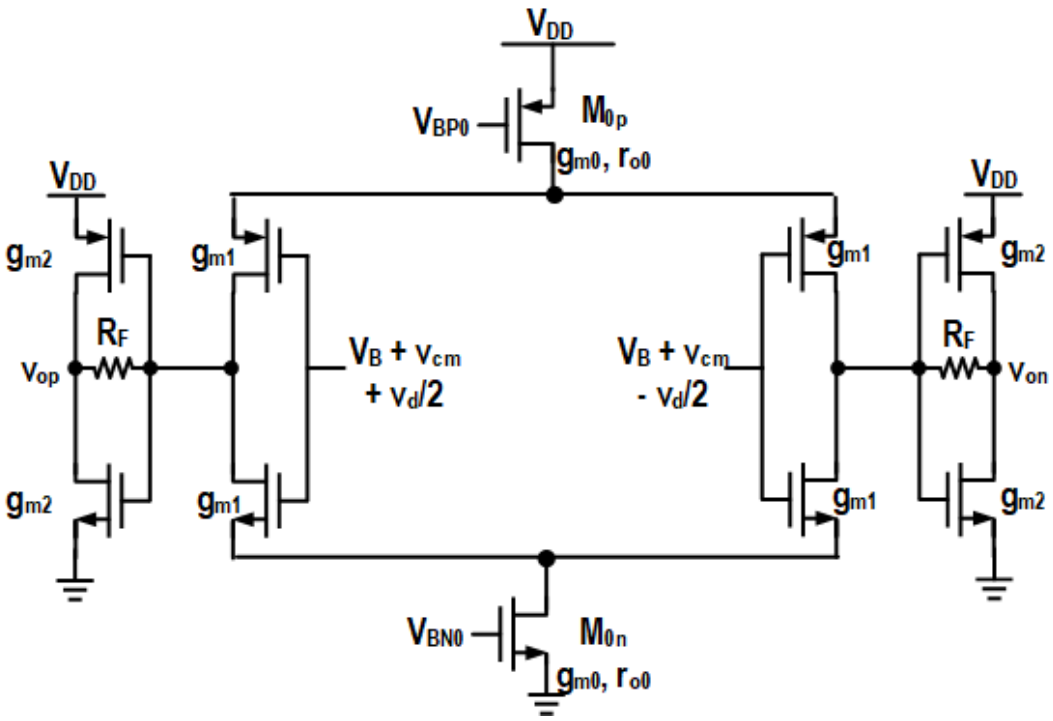
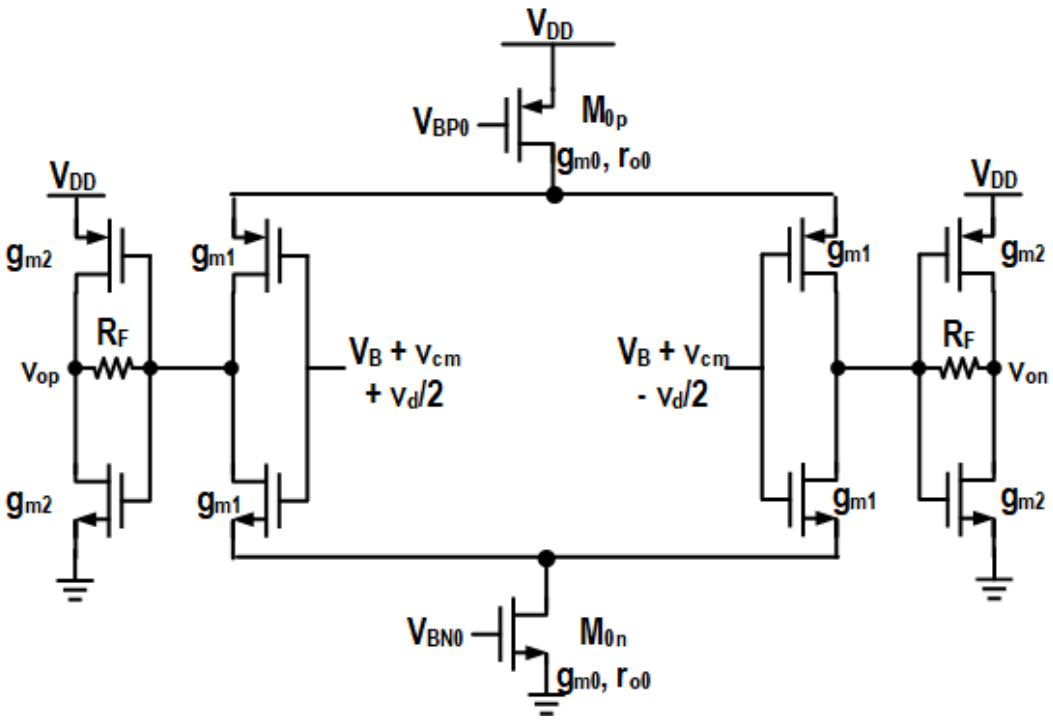


Figure 2: Fig. for Q2

2. In this problem, neglect channel length modulation for all transistors except M_{0n} and M_{0p}. Assume that V_B, V_{BN0} and V_{BP0} are chosen such that all transistors are in the saturation region of operation. Answers to this question must be in terms of the small-signal parameters marked adjacent to the transistors.

   (a) (5 points) Compute the small-signal differential gain $(v_{op} - v_{on})/v_d$.

Additional space to work out problem 2.



Neglect channel length modulation for all transistors except M_{0n} and M_{0p}. Assume that all transistors are in the saturation region of operation.

(b) (5 points) What is small-signal common-mode gain $\frac{v_{op}}{v_{cm}}$, which is also equal to $\frac{v_{on}}{v_{cm}}$?

Additional space to work out problem 2.

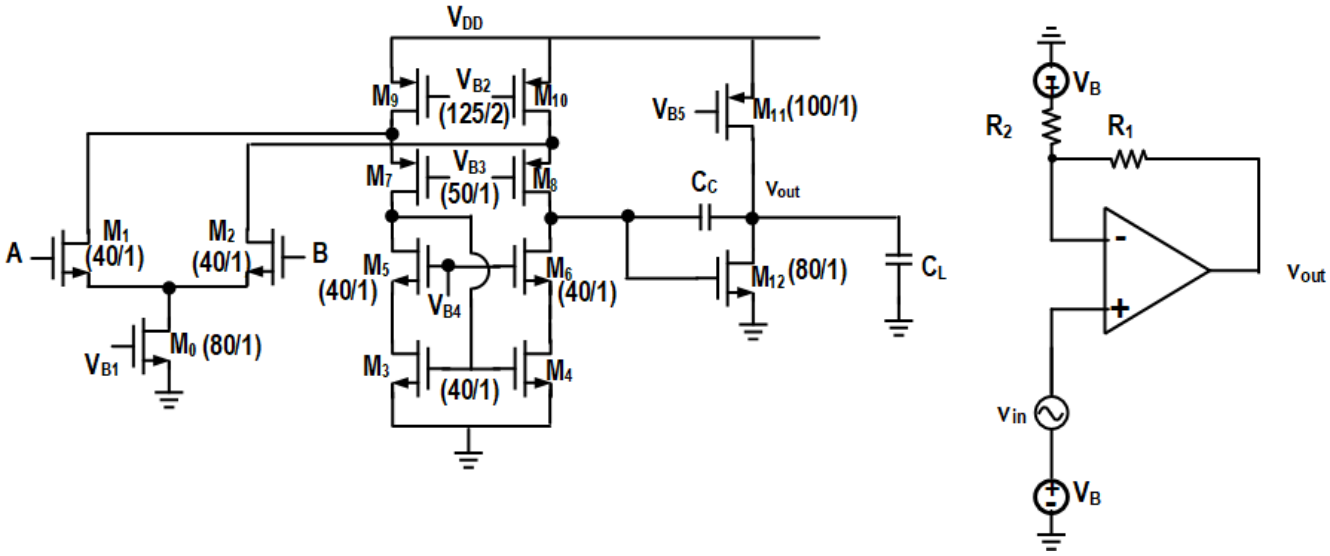


Figure 3: Fig. for Q3(a)

3. Assume $V_{DD} = 2V$, $V_{B1} = 0.4V$, $V_{B2} = 1.4V$, $V_{B3} = 1.2V$, $V_{B4} = 0.75V$, $V_{B5} = 1.4V$ for the two-stage op-amp in this question. Also, assume $C_C = 10pF$.

   (a) (5 points) Assume that the op-amp is connected as a non-inverting amplifier as shown in Fig. 3. Assume that $V_B = 1V$ and v_{in} is a sinusoid of the form $A\sin\omega_0 t$, where ω_0 is much smaller than the 3-dB bandwidth of the circuit. What is the maximum swing A for which all transistors remain in saturation. Assume that $R_1 = R_2$, $g_m r_o \gg 1$ for all transistors. Also, neglect effects of loading of the resistors R_1, R_2.

Additional space to work out problem 3.

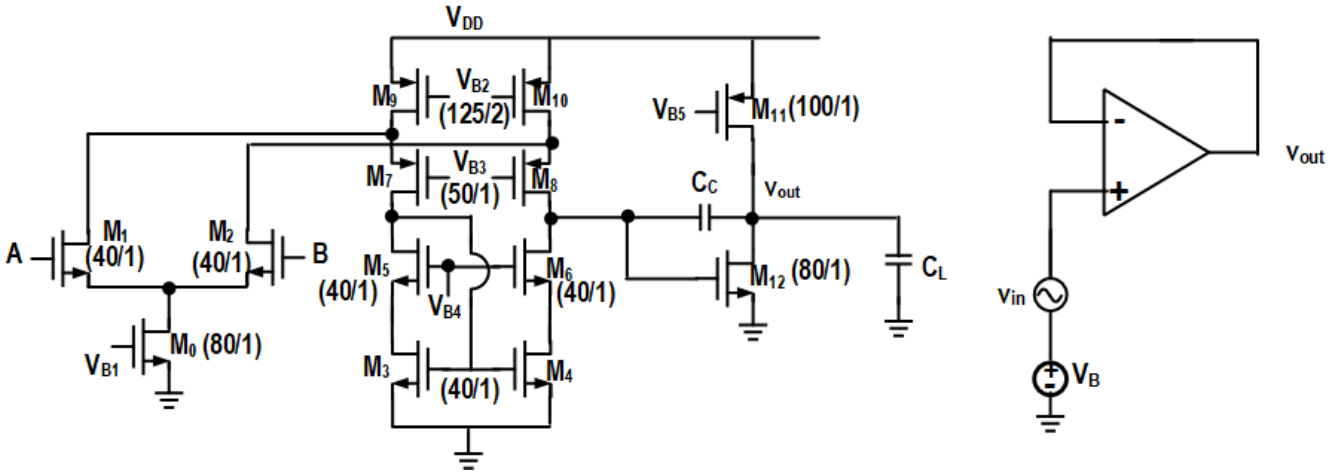


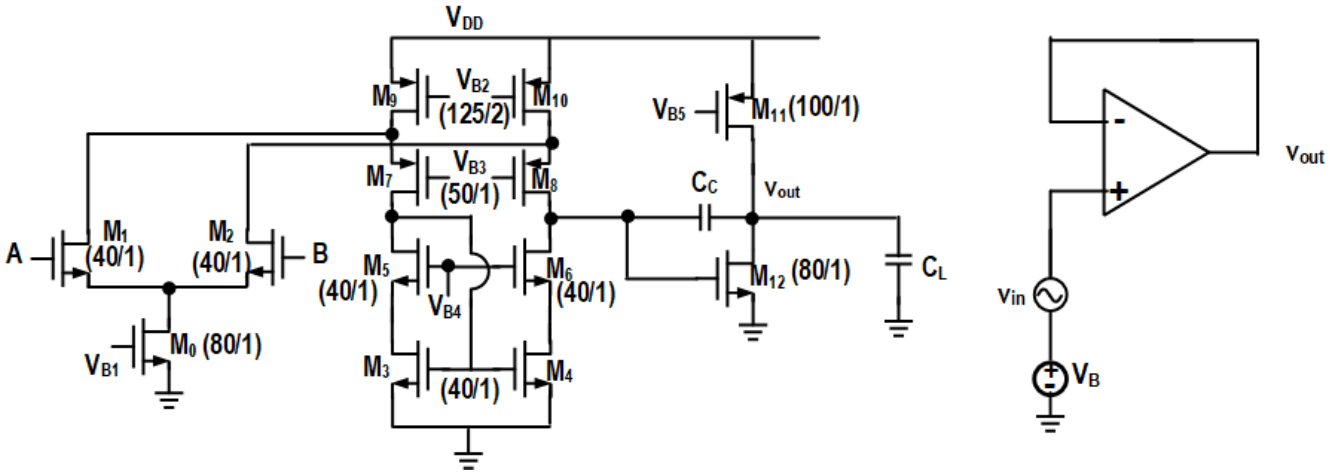
Figure 4: Fig. for Q3(b)-(e)

Assume $V_{DD} = 2V$, $V_B = 1V$, $V_{B1} = 0.4V$, $V_{B2} = 1.4V$, $V_{B3} = 1.2V$, $V_{B4} = 0.75V$, $V_{B5} = 1.4V$ for the two-stage op-amp in this question. Also, assume $C_C = 10pF$.

(b) (1 point) For the remainder of this question, assume that the op-amp is connected in unity gain feedback as shown in Fig. 4. To which node must the output node v_{out} be connected in the 2-stage op-amp, A or B?

(c) (5 points) Assume that the op-amp is connected in unity gain feedback as shown in Fig. 4. What is the maximum value of load capacitance C_L for which the output slew-rate is independent of the value of C_L?

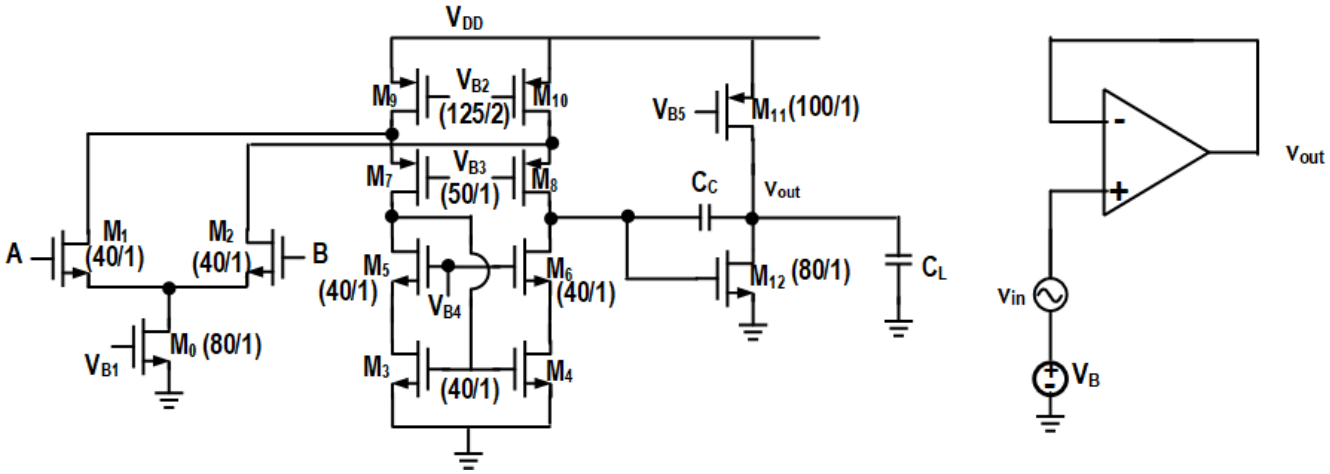
Additional space to work out problem 3.



Assume $V_{DD} = 2V$, $V_B = 1V$, $V_{B1} = 0.4V$, $V_{B2} = 1.4V$, $V_{B3} = 1.2V$, $V_{B4} = 0.75V$, $V_{B5} = 1.4V$ for the two-stage op-amp in this question. Also, assume $C_C = 10pF$. Assume that $C_L = 5pF$ for part (d).

(d) (4 points) Now, assume $C_L = 5pF$. v_{in} is a sinusoid of the form $Asin2\pi f_0 t$, where $f_0 = 10MHz$. What is the maximum input swing A for which the output is not slew-rate limited?

Additional space to work out problem 3.



Assume $V_{DD} = 2V$, $V_B = 1V$, $V_{B1} = 0.4V$, $V_{B2} = 1.4V$, $V_{B3} = 1.2V$, $V_{B4} = 0.75V$, $V_{B5} = 1.4V$ for the two-stage op-amp in this question. Also, assume $C_C = 10pF$. Assume that $C_L = 5pF$ for part (e).

(e) (6 points) In this part, assume $C_L = 5pF$. What is the unity gain frequency of the op-amp? Also, estimate the phase margin. You may assume $\lambda = 0.2/V$ for all transistors for this part.

Additional space to work out problem 3.

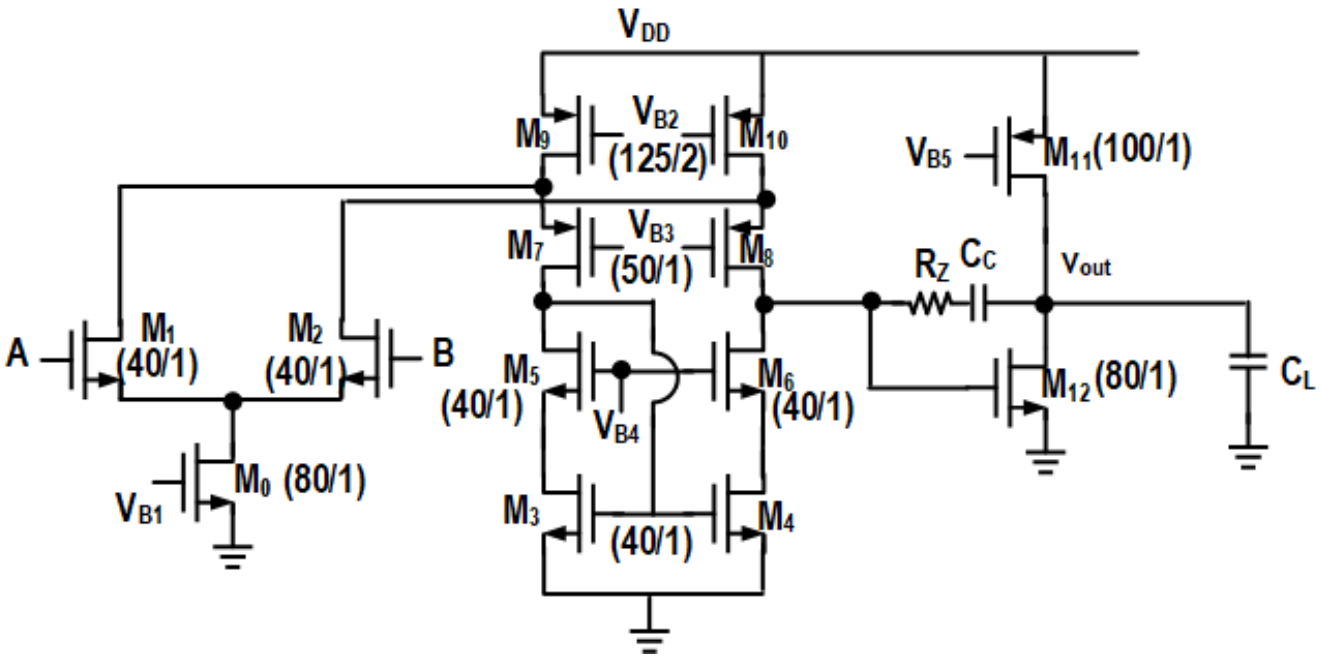


Figure 5: Fig. for Q3(f)

Assume $V_{DD} = 2V$, $V_B = 1V$, $V_{B1} = 0.4V$, $V_{B2} = 1.4V$, $V_{B3} = 1.2V$, $V_{B4} = 0.75V$, $V_{B5} = 1.4V$ for the two-stage op-amp in this question. Also, assume $C_C = 10pF$. Assume that $C_L = 5pF$ for part (f).

(f) (4 points) Now, a resistor is placed in series with C_C to cancel the zero in the frequency response of the two-stage op-amp. What is the value of R_z needed to cancel the zero?

Additional space to work out problem 3.

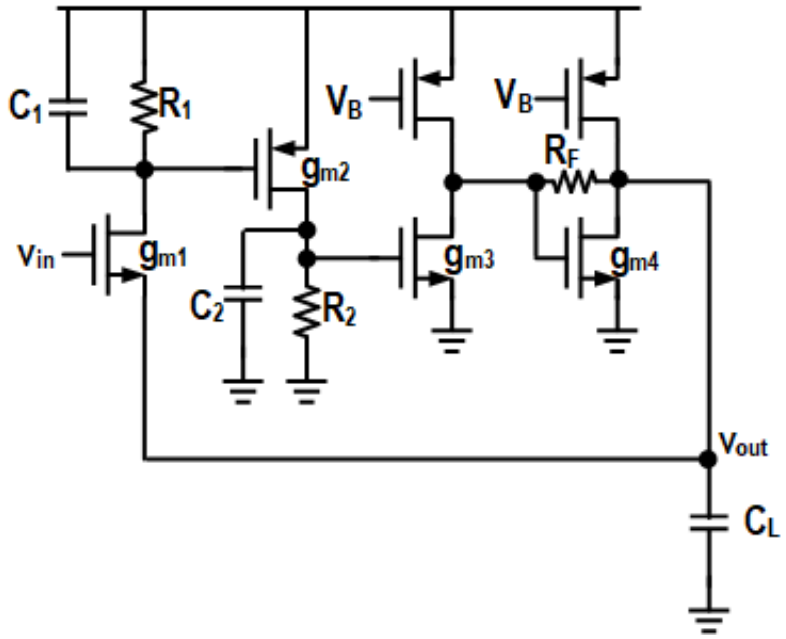


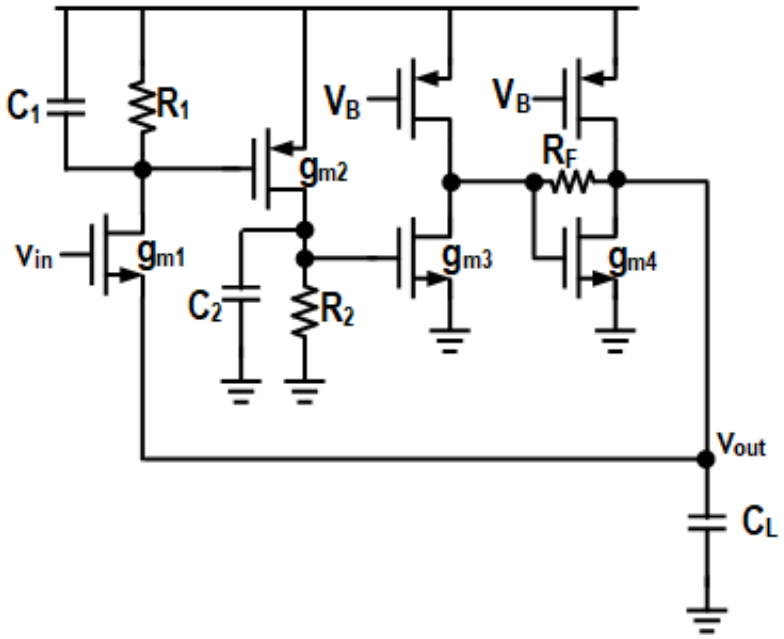
Figure 6: Fig. for Q4(a)

4. (a) (1 point) What is the type of feedback in this circuit at the input, series or shunt?

(b) (1 point) What is the type of feedback in this circuit at the output, series or shunt?

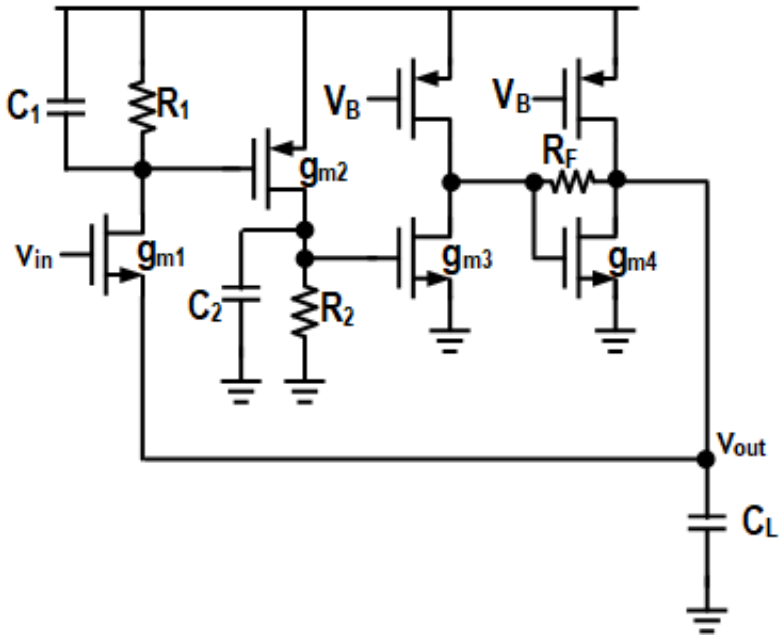
(c) (3 points) In this part, assume $g_{m1} = g_{m2} = 10\text{mS}$, $g_{m3} = 10\text{mS}$, $g_{m4} = 20\text{mS}$. $R_1 = R_2 = 1\text{k}\Omega$, $R_F = 250\Omega$. Using 2-port feedback techniques, evaluate the closed loop gain v_{out}/v_{in}. Assume $C_1 = C_2 = C_L = 0$ for this part.

Additional space to work out problem 4.



(d) (4 points) In this part, assume $g_{m1} = g_{m2} = 10\text{mS}$, $g_{m3} = 10\text{mS}$, $g_{m4} = 20\text{mS}$. $R_1 = R_2 = 1\text{k}\Omega$, $R_F = 250\Omega$. Using 2-port feedback techniques, evaluate the closed output impedance. Assume $C_1 = C_2 = C_L = 0$ for this part.

Additional space to work out problem 4.



(e) (6 points) In this part, assume $g_{m3} = 10\text{mS}$, $g_{m4} = 20\text{mS}$. $R_F = 250\Omega$, $\text{R}_1 = \text{R}_2 = 1\text{k}\Omega$. Assume $C_1 = C_2 = 100\text{fF}$, $C_L = 2\text{pF}$. Assume $g_{m1} = g_{m2} = g_m$. What is the maximum value of g_m for which the circuit is stable? (*Hint: Evaluate the loop gain of this third order system. Use the results derived in lecture regarding the stability of 3rd order systems.*)

Additional space to work out problem 4.

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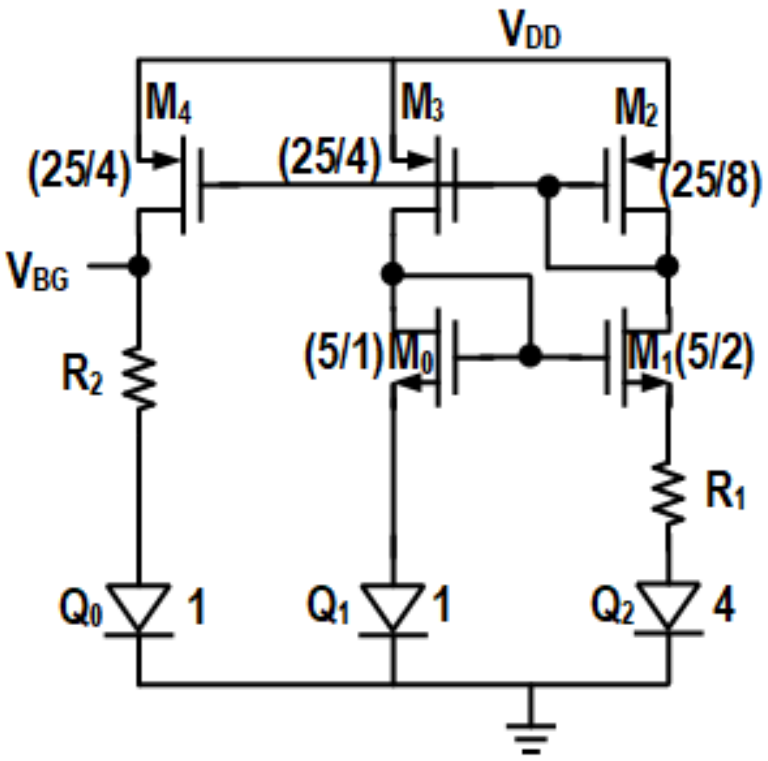
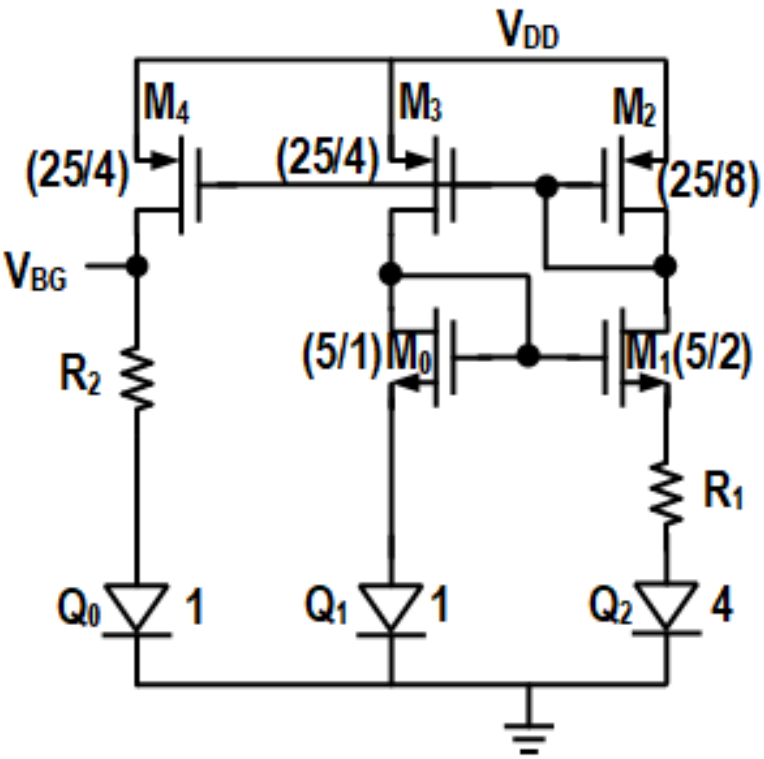


Figure 7: Fig. for Q5

5. Assume that the V_{BE} of the diodes Q_0, Q_1 is equal to 0.65V at 300K in this circuit. Assume $\frac{kT}{q} = 25\text{mV}$ at a temperature of 300K. Also, assume that the V_{BE} of the diodes Q_0, Q_1 has a temperature coefficient of -2mV/K. Assume that the resistor $R_1 = \ln(8)\text{k}\Omega$.

   (a) (5 points) For what value of R_2, will V_{BG} be a temperature-independent bandgap voltage? What is the value of this bandgap voltage? In this part assume $V_{DD} = 2\text{V}$.

Additional space to work out problem 5.



Assume that the V_{BE} of the diodes Q_0, Q_1 is equal to 0.65V at 300K in this circuit. Assume $\frac{kT}{q} = 25\text{mV}$ at a temperature of 300K. Also, assume that the V_{BE} of the diodes Q_0, Q_1 has a temperature coefficient of -2mV/K. Assume that the resistor $R_1 = \ln(8)\text{k}\Omega$.

(b) (4 points) What is the minimum supply voltage V_{DD} needed to achieve the bandgap voltage obtained in (a), without pushing any MOS transistor into the triode region of operation?

Additional space to work out problem 5.

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